Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Maejo International

Journal of Science and Technology

ISSN 1905-7873

Available online at www.mijst.mju.ac.th

Review

Recent trends in silicon carbide device research

Munish Vashishath[1,*] and Ashoke K. Chatterjee[2]

[1] Department of Electrical and Electronics Engineering, YMCA Institute of Engineering, Faridabad, India 121006

[2] Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, India, 147004

* Author to whom correspondence should be addressed, e-mail: [1]munish.vashishath@gmail.com

Received: 15 March 2008 / Accepted: 28 July 2008 / Published: 4 August 2008

Abstract: Silicon carbide (SiC) has revolutionised semiconductor power device performance. It is a wide band gap semiconductor with an energy gap wider than 2eV and possesses extremely high power, high voltage switching characteristics and high thermal, chemical and mechanical stability. The SiC wafers are available in 6H, 4H, 2H and 3C polytypes. Because of its wide band gap, the leakage current of SiC is many orders of magnitude lower than that of silicon. Also, forward resistance of SiC power devices is approximately 200 times lower than that of conventional silicon devices. The breakdown voltage of SiC is 8-10 times higher than that of silicon. In this paper, silicon carbide Schottky barrier diodes, power MOSFETs, UMOSFET, lateral power MOSFET, SIT (static induction transistor), and nonvolatile memories are discussed along with their characteristics and applications.

Keywords: silicon carbide, power MOSFET, SIT, nonvolatile memory

---

Introduction

Silicon carbide (SiC) is the only WBG (wide band gap) semiconductor that possesses a high-quality native oxide for use as an insulator in electronic devices. The main advantage of silicon carbide is that it can resist high field strengths and offers better heat conducting capacity than copper at room temperature. Due to high thermal conductivity and high breakdown electric field strength, SiC can be used at high temperature, high voltage, high frequency and high power applications. Table 1 gives the comparison of the electrical properties of SiC with other semiconductors, viz. Si, GaN and GaAs.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Table 1. Comparison of electronic properties of SiC with Si, GaAs and GaN

	Si	**GaAs**	**GaN**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field @ $10^{17}cm^{-3}$(MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron mobility @$10^{16}cm^{-3}$ (cm^2/V-s)	1100	6000	1000	370	800	750
Hole mobility @$10^{16}cm^{-3}$ (cm^2/V-s)	420	320	200	90	115	40
Saturated electron drift velocity (cm/s)	10^7	10^7	$2.5x10^7$	$2x10^7$	$2x10^7$	$2.x10^7$
Intrinsic concentration, n_i (cm^{-3})	$1.5x10^{10}$	$1.9x\ 10^{-10}$	$2.1x10^6$	$2.3x\ 10^{-6}$	$8.2x\ 10^{-9}$	6.9
Thermal conductivity	1.5	0.55	1.3	4.9	4.9	5

(After R. Y. Lakhshman, MS Thesis, Mississippi State University, 2001, Ref. 8)

Thermal oxidation of SiC produces a layer of SiO_2 on the surface while the carbon atoms from the SiC form CO, which escapes as gas. Thus, it is possible to make all devices found in silicon IC technology in SiC, including high quality, stable MOS transistors and MOS integrated circuits. Examples of WBG semiconductors are: gallium nitride (GaN, E_G=3.4eV), aluminum nitride (AlN, E_G = 6.2eV) and silicon carbide (SiC, E_G between 2.2-3.25 eV depending on the polytype used). SiC is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature. Finally, SiC is the only compound semiconductor which can be thermally oxidised to form a high quality native oxide (SiO_2). Although SiC offers substantial advantages over silicon, it is still immature as a semiconductor material. The main limitations of the technology are in the area of crystal growth.

In 1955, a laboratory simulation process for growing SiC crystals was developed by J. A. Lely [1]. In the Lely process, the nucleation of individual crystals are uncontrolled and the resulting crystals are randomly sized hexagonal-shaped a-SiC platelets. In 1978, Tairov and Tsvetkov [2] introduced the growth of SiC single crystals by the vapour transport process.

In 1983, Ziegler [3] introduced the modified sublimation process for growing SiC single crystals. In 1987, a research group under R. F. Davis at North Carolina State University (NCSU) announced a modification to the original Lely sublimation process [4]. In this modified process, only one large crystal is grown and this crystal consists of a single polytype. In this process, which is the basis of current commercial systems, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at 200 Pa.

In 1987, the students from the NCSU group founded a small company, Cree Research, to produce silicon carbide commercially. Single crystal SiC forms in the hexagonal lattice, with alternating hexagonal planes of silicon and carbon atoms. Each silicon atom bonds to four nearest-neighbouring carbon atoms and each carbon atom is attached to four nearest-neighbouring silicon atoms. Doping of silicon carbide can be done during epitaxial layer growth or after crystal growth by ion implantation.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

But ion-implantation is normally used because of lower quality due to crystal damages created during ion bombardment than doped epilayers. The first step in making silicon carbide semiconductor devices is to grow the epitaxial layer using a process called chemical vapour deposition (CVD). The silicon carbide epilayers are produced in the CVD process by thermally decomposing silicon and carbon source gases (called precursors) onto boule-derived SiC substrates.

The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different polytypes of the material identified by the repeating distance of the stacking sequence (e.g. 3C,4H & 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as band gap energy, electron mobility and critical field differ significantly between the polytypes [5-7].

The electrical properties are changed by adding impurities and the impurity elements affect the electrical properties. The control over the impurity addition in CVD SiC epilayers is very limited. This leads to difficulties over the control of unintentional impurities, which makes it difficult to control and achieve the desired epilayer thickness. The other method of doping silicon carbide is selective doping after epitaxial layer formation. The selective doping is accomplished by ion implantation; the diffusion coefficients of aluminium and nitrogen are so low that diffusion in silicon carbide is impossible. Diffusion in SiC at high temperatures produces significant surface damage. Successful fabrication of implanted layers in SiC depends on the proper choice of implant anneal conditions. Implant activation typically requires annealing at temperatures between 1000 and 1700 °C.

Chemical etching is impractical owing to the high chemical stability of SiC and selective etching is accomplished by reactive ion etching (RIE) using fluorinated gases. SiC offers significant advantages for power electronics applications such as lamp ballasts, motor control, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits.

There are a number of possible crystal structures. These are 2H, 3C, 4H and 6H; but the most important are 3C, 4H and 6H. These structures differ by band gap energy, carrier mobility and breakdown field. For example, the energy gaps are 2.2, 3.26 and 3.0 eV for 3C, 4H and 6H-SiC respectively.

In this paper silicon carbide Schottky barrier diode, power MOSFET, lateral power MOSFET, static induction transistor and nonvolatile memory are discussed along with their characteristics, uses, structures and applications. Table 2 gives performance details of commercially available silicon carbide-based devices which are developed by Purdue Group, Cree Group, Rutgers/USCI and Denso Group.

Silicon Carbide Schottky Barrier Diode

Schottky barrier diodes (SBD) are unipolar devices, i.e. they do not inject minority carriers into a neutral region as do PN diodes. Since there is no minority charge storage, the turn of event is fast and the transient reverse current is small. As a result, the switching energy dissipated during turn-off is minimal. Hence, Schottky diodes eliminate the switching losses. SiC Schottky barrier diodes are attractive because the breakdown field of SiC is 8 to 10 times higher than for silicon. Hence, these are

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Table 2. The best-reported SiC based power devices such as Schottky barrier diodes and power MOSFETS [83] fabricated and tested by different groups

Diode					
Sr. No.	**Fabricated Device**	**Blocking Voltage (KV)**	**Specific on resistance mΩcm^2**	**Figure of merit (MW/cm^2)**	**Device Fabricated By**
1	Schottky Barrier Diodes	4.9	43	558	Purdue Group
2	JBS Diode (4H)	5.96	24	1,480	Rutgers
3	Schottky Diode (4H)	10.8	97	1,202	Rutgers / USCI
4	MPS Diode (4H)	4.38	20.7	928	Rutgers / USCI
5	MPS Diode (4H)	1.5	10	225	Cree, Inc.
MOSFETs					
1	DMOSFET (6H)	.760	125	4.62	Purdue Group (1996)
2	DMOSFET	.350	18	6.81	NCSU (1997)
3	DMOSFET (4H)	2.4	42	137	Cree, Inc.
4	UMOSFET	1.41	275	7.2	Cree Group (1997)
5	IOP-UMOSFET (4H)	1.4	15.7	125	Purdue Group (1998)
6	UMOSAFET	.45	10.9	18.6	Denso Group (1997)

capable of operation at much higher temperatures than silicon devices. Purdue University fabricated the 1700V 4H-SiC Schottky barrier diode using both Ni and Ti as Schottky metals. Figure 1 shows the cross section of SBD. The N-layer is 10-13 microns thick.

The semiconductor under the edges of the Schottky contact is implanted with boron. Under reverse bias this produces a region containing a large density of deep levels that serve as charge trapping centres and accumulate a distributed charge that reduces the electric field crowding at the edges of Schottky contact [9]. The Schottky metal is covered with 1 micron of gold metallisation to reduce spreading resistance of the Schottky contact and the backside ohmic contact is formed by annealed nickel.

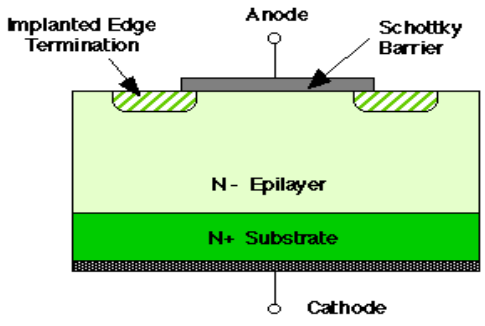

Figure 1. Cross section of SBD
(After A. Itoh et al., Ref. 9)

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Figure 2 shows the forward and reverse (V-I) characteristics for the Ti and Ni contacted SBD. The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 eV and 1.3 eV respectively and the lower barrier Ti gives lower forward voltage drop but higher leakage current as compared to the Ni barrier. The reverse blocking voltages are 1500 and 1720 volts respectively.

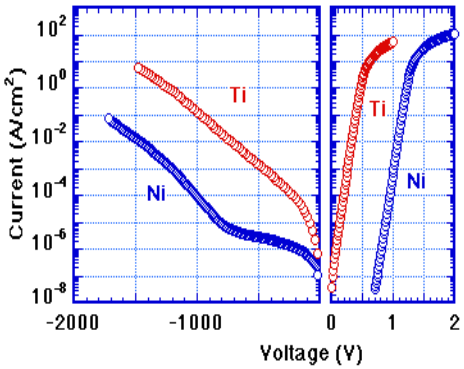

Figure 2. Forward and reverse (V-I) characteristics of SBD with Ti and Ni (After A. Itoh et al., Ref. 9)

Status of SiC based Schottky barrier diodes

In 1996, 4H-SiC Schottky barrier diodes having 1400 V with forward current densities over 700 A/cm^2 at 2 V were demonstrated [10]. In this paper, the Schottky rectifier consists of an N+ doped substrate (thickness ~11 mil) with back-side ohmic contact, a lightly doped (1x10^{16} cm^{-3}) epitaxial drift layer (thickness ~10 µm), and a top-side Schottky contact with a high-resistivity edge termination. The Schottky diode is fabricated by evaporating a high work function metal such as titanium, nickel, or gold, onto the epitaxial layer to form the Schottky contact and by depositing an ohmic contact metal onto the back of the N+ substrate.

In 1997, the results obtained with limited area amorphisation by argon ion-implantation at the periphery of 6H SiC Schottky barrier diodes were reported [11]. A variety of edge termination structures based upon the amorphised implanted region were studied during this work. The termination structures were fabricated using a three-mask process to create a high resistivity layer at the periphery of the device formed by using high dose argon ion-implantation with its position and area defined using a photoresist mask. It was established that, for obtaining a high breakdown voltage, the high resistivity layer should be in contact with the Schottky metal. It was demonstrated that only 50µm of the implant region is required at the periphery to obtain ideal plane parallel breakdown voltages. The leakage current at small reverse bias voltages was found to be directly proportional to the implant area.

In 2000, an accurate modeling and complete parameter extraction of the forward characteristics of the Ni/6H SiC Schottky barrier diodes (SBD) for high level current densities were presented [12]. The model took into account the high level injection effects of the excess majority carriers and current dependence of the series resistance. Direct extraction of the large bias SBD parameters was carried out. A very good agreement between the simulated forward curves using extracted parameters and measured data up to 500 A/cm^2 was obtained.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

In 2001, the static and dynamic characteristics of large-area, high-voltage 4H-SiC Schottky barrier diodes were presented [13]. This device achieved the breakdown voltage greater than 1200 V and a forward current of 6 A, and enabled the use of SiC Schottky diodes in practical switching circuits.

In 2001, accurate modelling and parameter extraction for 6H-SiC Schottky barrier diodes with nearly ideal breakdown voltage were demonstrated [14]. Ni Schottky rectifiers on $2.7x10^{16}$ cm^{-3} n-type 6H-SiC epilayer using an effective edge termination based on an oxide ramp profile around the Schottky contact got experimented and simulated. Several anneals of the Schottky contacts were experimented. In particular, the diodes annealed at 900 ºC showed excellent reverse characteristics with a nearly ideal breakdown at about 800 V. In this work the device simulation was performed in MEDICI simulator.

In 2001, the use of thermally evaporated Ti Schottky barrier diodes on n type 6H SiC was fabricated [15]. They showed good rectification characteristics at room temperature. These diodes demonstrated a low reverse leakage current of below $1x10^{-4}$ A/cm^2. Using neon implantation to form edge termination improved the breakdown voltage up to 800 V.

In 2002, a new junction termination structure named guard ring assisted RESURF was proposed [16]. The structure maintained a stable and high breakdown voltage without being influenced by the deviation of impurity dose in the RESURF layer or by parasitic charge. The GRA-RESURF structure was adopted on 600-V range 4H-SiC Schottky barrier diodes and achieved high breakdown voltages with a good production yield in a wide range of implanted dose from $1x10^{13}$ to $5x10^{13}$ cm^{-2}. Comparison of various termination structures was also discussed in this paper.

In 2003, the breakdown voltage of 10 kV based on a 115μm n-type epilayer doped to $5.6x10^{14}$ cm^{-3} through the use of a multistep junction termination extension was demonstrated on 6H silicon carbide wafer [17]. A current density of 48 A/cm^2 was achieved with a forward voltage drop of 6V.

In 2004, the effect of different mechanism on the characteristics of silicon carbide characteristics was discussed [18]. In this paper, a number of experiments demonstrated that the Schottky barrier height for metal-SiC is different from the theoretical prediction. On the basis of non-uniform barrier height assumption for metal-SiC contact, a numerical simulation with 2D simulator MEDICI was performed in this paper. The simulation results showed that the model matches the experimental data very well. Patch defects make the Schottky-barrier height decrease. This may give a reasonable explanation for the non-ideal behaviours observed from many experiments. The effect of interface state density on Schottky barrier height was also discussed.

In 2005, high-voltage and low-loss 4H–SiC Schottky barrier diodes with a performance close to the theoretical limit using a Mo contact annealed at high-temperature were fabricated [19]. High-temperature annealing for the Mo contact was found to be effective in controlling the Schottky-barrier height at 1.2–1.3 eV without degradation of n-factor and reverse characteristics. Breakdown voltage of 4.15 kV, specific on-resistance of 9.07 $m\Omega cm^2$ and figure of merit of 1898 MW/cm^2 were achieved and also obtained were a 9 mm^2 Mo–4H–SiC SBD with breakdown voltage of 4.40 kV and specific on-resistance of 12.20 $m\Omega cm^2$ in this paper.

In 2005, the performance of the commercially available and recently fabricated Schottky barrier diode of breakdown voltage of 1.2 kV was compared with the Si diodes at high temperature [20]. It was found that for a rated breakdown voltage of 1.2 kV, SiC Schottky diodes offer better performances in terms of switching time and recovery charge than PN-Si ultra-fast diodes, although they show slightly

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

higher forward voltage drops. Lower reverse leakage current was obtained using Ni instead of Ti for the Schottky contact.

In 2006, a new high voltage 4H-SiC SBD structure for monolithic microwave integrated circuit (MMIC) applications was proposed [21]. It employed one or more floating metal rings (FMR) which work in a similar fashion to guard rings. The influence of FMR structure on the breakdown voltage and cut-off frequencies of the SBD was studied by numerical device modeling. As compared to the one without ring, about 107% and 134% improvement in breakdown voltage while only about 17% and 25% decrease in cut-off frequencies was achieved in SBD with one and two rings.

Power MOSFET

Power switches can be considered as the heart of all power electronic systems. The increased power capabilities, ease of control, and reduced costs of power switches have made power electronic systems affordable in a large number of applications. The first power switches were thyristors and bipolar transistors. Thyristors were used in higher power systems because their ratings were scaled at a faster pace than bipolar transistors. Bipolar transistors were favoured for low and medium power applications because of their faster switching capability. The rating of these devices grew steadily until the late 1970s, the years in which the first power MOSFETs were introduced. Since the introduction of the first power MOSFETs, Si power MOSFETs have been immensely improved and have become the dominant device technology since 1980s for many applications for many reasons. First, MOSFET has a very high input impedance due to its MOS gate structure. Hence, it provides the simplest gate drive requirements. The creation of either inversion layers or accumulation layers under the MOS channel can be controlled using integrated circuits because of the small gate current that is required to charge and discharge the high input gate capacitance. Second, the MOSFET is a majority carrier device hence there is no minority charge storage involved in its operation. This results in faster switching operation. Third, compared to the bipolar transistors the MOSFETs have superior ruggedness and forward biased safe operating area which allows the elimination of snubber circuits for protection of the switch during operation in typical hard-switching applications. Fourth, as the majority carriers in silicon exhibit increasing resistivity with temperature, the thermal runaway behaviour is avoided in MOSFETs. MOSFET devices are formed as parallel combination of many thousands of individual MOSFET cells to take advantage of the thermal behaviour. Any device carrying excess current will heat up and become more resistive, diverting current into parallel paths. Excessive loss still produces thermal failure in MOSFET, but there is no unstable runaway effect if the parasitic BJT does not act. Due to these excellent characteristics, it would be desirable to utilise power MOSFETs for high voltage/power electronic applications. However, the blocking voltage capability of the MOSFET is based upon the ratings of the reverse body diode of the drift region. This blocking voltage is determined in part by the distance from source to drain. High blocking voltage capability implies high resistance because of geometry, so there is a trade-off between low drift region resistance and diode voltage capability.

Comparison of the figure of merits of Si and SiC polytypes determined by various scientists is given in Table 3. On the basis of Keyes' and Johnson's figure of merits, SiC has superior properties as compared to Si. They derived the figure of merits for high speed switches and high power discrete amplifiers. The figure of merits emphasises the electrical and thermal properties of various

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

semiconducting materials for evaluating their power handling capability. Baliga derived two figures of merits. One is for low frequency and the other is for high frequency as well as high-power unipolar switches.

Table 3. Comparison of figures of merits SiC with Si [84]

Figure of Merits	**Si**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Johnson's FOM	1	400	400	280
Keyes' FOM	1	5.1	5.1	5.8
Baliga FOM (Low Frequency)	1	240	560	140
Baliga FOM (High Frequency)	1	29	69	25

Silicon carbide based MOSFET can be used in high power applications and hence it requires a high breakdown voltage. The one-step field plate termination can enhance the breakdown voltage to 910 V, embedded mesa termination can increase it to 1350 V, and the embedded mesa with step field plating can give a breakdown voltage of 1100 V [22]. However, 6H-SiC DIMOSFETs in practice have attained a maximum blocking voltage of 760 V [23]. The specific on-resistance of the drift region of the MOSFET can be significantly reduced by enhancing the inversion channel mobility using pyrogenic re-oxidation annealing [24], thereby reducing the power dissipation.

Power MOSFET can be classified under the following headings:

(i) Double implanted or DIMOSFET

(ii) UMOSFET

(iii) Lateral or LDMOSFET

Double implanted MOSFET

Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only by using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO_2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC. Here we will discuss double implanted MOS (DMOS) as shown in Figure 3. DMOS transistors are

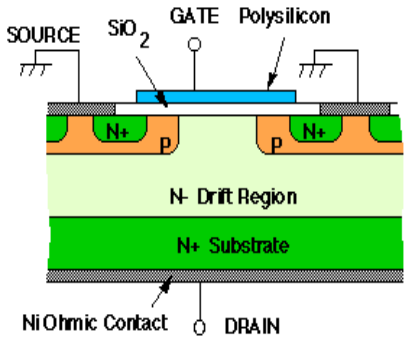

Figure 3. Double implanted MOSFET
(After J. N. Shenoy et al., Ref. 26)

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

common in silicon power device technology where the p-base and n^+ source regions are formed by diffusion of impurities through a common mask opening [25]. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n^+ source [26-29]. The implanted DMOSFET requires that separate masks be used to define the p-base and the n^+ source. The construction is a vertical structure with a drift layer built on a highly conductive n^+ layer. The n-drift region is designed to give the forward blocking capabilities (Figure 3). The forward blocking capability is achieved by the pn junction between p-base region and n-drift region. During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n^+- source region. By short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides. However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region. On applying the positive bias to the gate electrode, the conductive path between the n^+-source region and the n-drift region is formed. The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components. The total specific on-resistance [30] is determined as

$$R_{on\text{-}sp} = Rn^+ + R_C + R_A + R_J + R_D + R_S \qquad (1),$$

where $R_{on\text{-}sp}$ is the specific on-resistance, Rn^+ is the contribution from the n^+ -source, R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base regions by virtue of the JFET pinchoff action, R_D is the drift region resistance and R_S is the substrate resistance. In a power MOSFET, the blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n^+-source, the n-channel, the accumulation region and the n^+-substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating $R_{on\text{-}sp}$. However, at higher break down voltages, R_D is significantly higher than other resistances and $R_{on\text{-}sp}$ can be approximated by R_D. The drift region analysis for an ideal DIMOSFET structure can be performed by taking the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor. The doping level $N_B\,(cm^{-3})$ required to support a given breakdown voltage V_B and the depletion width W(cm) [31] can be given by

$$N_B = \frac{\varepsilon E_C^2}{2qV_B} \qquad (2);$$

$$W = \frac{2V_B}{E_C} \qquad (3).$$

The specific on-resistance associated with the drift layer to support V_B [32] is given by

$$R_{on-sp} = \frac{W}{qN_B\mu_n} \qquad (4).$$

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Substituting (2) and (3) in (4), we get

$$R_{on-sp} = \frac{4V_B^2}{\varepsilon E_C^3 \mu} \qquad (5),$$

where ε is the permitivity in F/cm, E_C is the breakdown field in V/cm, q is the electronic charge in C and μ_n is the electron mobility in cm^2/V-sec [33]. From the equations, it has been confirmed that both the mobility μ_n and breakdown field E_C depend on N_B. The (V-I) characteristics of DIMOSFET are shown in Figure 4.

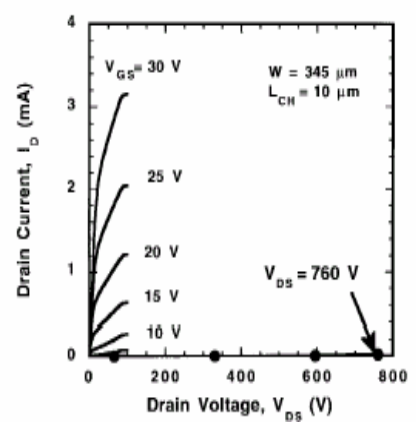

Figure 4. (V-I) characteristics of DIMOSFET
(After M. Bhatnagar and B. J. Baliga, Ref. 30)

SiC DIMOSFETs have been fabricated with the blocking voltage of 760V. To obtain the blocking voltage greater than 760 V for 6H-SiC depends on the drift region thickness, doping level, specific on-resistance and electric field strength. By adjusting all these parameters we propose to get the blocking voltage greater than 760V.

The safe operating area of MOSFET is divided into three regions: (i) maximum permissible drain current, (ii) maximum power dissipation limit, and (iii) maximum drain source voltage limit. The safe operating area of MOSFET does not contain any second breakdown as seen in the BJT. This is because of the majority carriers present in the MOSFET.

UMOSFET

The UMOSFET is formed by reactive ion etching, the electrical fields at the bottom corners being lower than that at the tip of the V- groove MOSFET. The substrate acts as the drain electrode. It is lightly doped and thick, constituting the lightly doped drain to ensure a high blocking voltage. The p-type base layer is grown by epitaxy and is grounded. As shown in Figure 5 the UMOS forms the pn junction and the MOS channel. In the blocking state the gate is grounded, which turns the MOS channel off. The large drain voltage is supported by the reverse-biased junction and the MOS capacitor. The electric fields in the pn junction and the MOS capacitor are shown to the right of the figure. It has been observed that the electric field in the oxide at the trench bottom is 2.5 times higher than the peak field in the semiconductor. Such high fields may lead to the damage of the oxide before the pn junction breaks

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

down. The field at the trench corners is even higher due to two-dimensional effects. Hence, in UMOSFETs the maximum blocking voltage depends on oxide breakdown and not on the semiconductor breakdown [34]. The maximum breakdown voltage provided by the device is 260V.

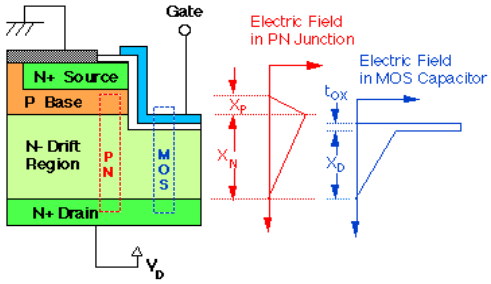

Figure 5. Cross section of 4H-SiC UMOSFET
(After J.Tan et al., Ref. 34)

In order to overcome the limitation of the device a new UMOSFET with integral oxide protection has been developed, which limits the electric fields in the trench which simultaneously reduces the on-resistance. The structure is shown in Figure 6 with electric fields in the blocking state. A new p-region is formed at the bottom of the trench by ion-implantation and reduces the electric field at the oxide/semiconductor interface to zero. A new n-type layer (known as current spreading layer) grown epitaxilly between the n-drift region and the p-type base layer prevents the pinch-off of the conducting channel in the on state. The layer also facilitates lateral current flow into the drift region. Figure 7 shows (V-I) characteristics of IOP-UMOSFET. The features of IOP-UMOSFET are as follows:

- The blocking voltage of the device is 1.4KV;
- The breakdown is nondestructive and the oxide failure does not occur;
- The specific on-resistance is 15.7 $m\Omega cm^2$; and
- The figure-of-merit $V_B^2/R_{on\text{-}sp}$ is 125 MW/cm^2, the highest value ever reported for a power MOSFET in any material system and 25 times higher than the theoretical limit for silicon power MOSFETs.

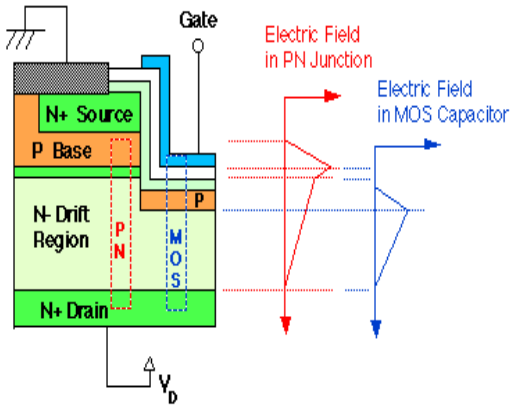

Figure 6. Cross section of 4H-SiC IOP-UMOSFET
(After J. Tan et al., Ref. 34)

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

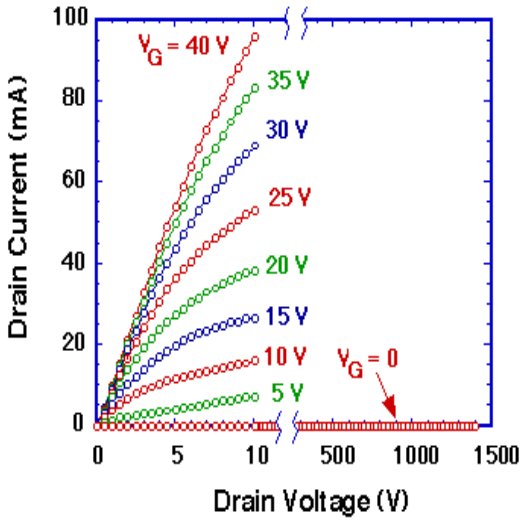

Figure 7. (V-I) Characteristics of IOP-UMOSFET
(After J. Tan et al., Ref. 34)

Lateral MOSFET

Before the advent of power devices of SiC, MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was blocked by a reverse-biased pn junction. In order to achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. In order to overcome the limitations of vertical-type MOSFETs we use the lateral-type MOSFET [35]. The structure of lateral DMOSFET is as shown in Figure 8. From the figure it can been observed that the insulating substrate is of SiC. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer. Figure 9 shows the current voltage characteristics of lateral DMOSFET. From the characteristics, it is observed that the device withstands a maximum drain voltage of 2.6 kV. From the above discussion we can say that the device should be implemented laterally rather than vertically because there is no necessity for an increase of surface area required for the device.

Problems in characterising the oxides in SiC MOSFET and MOS reliability

Silicon carbide MOS interface is more complex than that on Si due to the presence of carbon in the compound and the non-cubic crystal structure. The wide bandgap of SiC makes it difficult to measure the interface state density using MOS techniques at room temperature. This is due to the fact that interface states are more than about 0.6 eV from the majority carrier band exchange charge. Several MOS measurement techniques may be used for silicon carbide. Precautions must be taken to ensure that the interface states are actually responding. There are two effective methods which are used for

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

measuring the interface state density and these are the simultaneous hi-lo CV technique and the ac conductance technique.

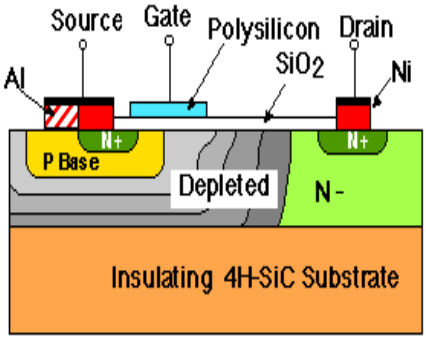

Figure 8. Cross section of lateral MOSFET
(After J. Spitz et al., Ref. 35)

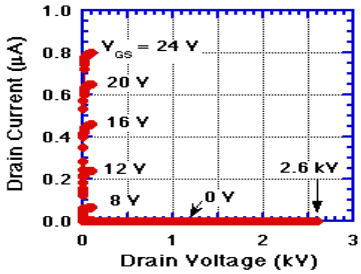

Figure 9. (V-I) Characteristics of lateral DMOSFET at room temperature
(After J. Spitz et al., Ref. 35)

SiC has a high-quality thermal oxide (SiO_2), thus it is possible to fabricate MOS-based power switching devices having extremely high input impedance. The limiting factor in these devices is likely to be the reliability of the thermally grown oxide. In order to achieve acceptable device reliability, the maximum field in the oxide may need to be limited. Unless this occurs, the high-field capability of SiC cannot be fully utilised. The reliability is evaluated using a MOS capacitor structure. Oxides are thermally grown by wet oxidation at 1150 °C using a baseline procedure that yields the interface state densities around 1.5×10^{11} eV^{-1} cm^{-2} and the fixed oxide charge densities around 9×10^{11} cm^{-2}.

Status and issues regarding the analysis and development of SiC based MOSFETs

In late 1980s, it was observed that power silicon devices were approaching their theoretical limits and that these limits could be significantly extended by fabricating power devices in the materials with higher breakdown electric fields, such as silicon carbide [36]. For vertically oriented majority carrier devices, the theoretical minimum value of the resistance-area product under punch- through condition is:

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_s E_C^3} \qquad (6)$$

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

where $R_{on\text{-}sp}$ is the specific on-resistance in Ωcm^2, μ_n is the electron mobility perpendicular to the surface, ϵ_s is the permittivity of the semiconductor, E_c is the critical field for avalanche breakdown perpendicular to the surface, and V_B is the designed blocking voltage of the drift region. Although it varies with doping, the critical field E_c in SiC is almost an order of magnitude higher than in silicon. Even allowing for the lower electron mobility, the specific resistance in SiC at a given blocking voltage is about 400 times than that in silicon.

In 1994, silicon carbide MOS characteristics were explained in a paper by Brown et al. [37]. This paper produced data which characterise the SiC/SiO_2 interface and explain one of the previously unexplained abnormalities observed in the characteristics of SiC MOSFETs. The outstanding distinction between the MOS characteristics on p and n type SiC wafers obviously indicates that the difference is probably caused by the fact that the p type wafers are Al doped and the n type wafers are N doped. The redistribution of impurities that occurs during the thermal oxidation of SiC and Si behaves in a similar fashion. N type dopants are rejected by the oxide during growth whereas p type dopants are incorporated into the oxide**.** Hence, the Al dopant in the oxide is likely to be the causes of the p type SiO_2/SiC interface characteristics [37].

The first MOSFETs in SiC were reported in the late 1980s and the first power MOSFETs in 1994 [38]. The power devices were the vertical-trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs were reported to have two serious problems: (a) A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage, and (b) The low inversion layer mobility along the trench sidewalls results in high specific on-resistance, which nullifies the advantage of low drift region in SiC. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

In 1996, the advantages and limitations of 4H-SiC power UMOSFET structure were demonstrated by US Air Force (WPAFB, Dayton Ohio) and Office of Naval Research, Arlington, Virginia [39]. According to this report, the use of p+ polysilicon gate leads to a higher breakdown voltage as the Fowler Nordheim injection from the gate electrode is reduced. It was also concluded that the insulator reliability is the limiting factor and therefore the high temperature operation of these devices may not be practical.

In 1997, Denso Corporation Japan introduced UMOSFET. This UMOSFET produced a blocking voltage of 450V, a specific resistance of 10.9 $m\Omega cm^2$, and $V_B^2/R_{on\text{-}sp}$ of 18.6 MW/cm^2 [40]. In the same year, Northrop Grumman Science and Technology Centre introduced and fabricated the 4H-SiC UMOSFETs at the blocking voltages of 1.1kV and 1.4 kV [40-41], as well as the 4H-SiC DIMOSFETs at a blocking voltage of 900V [42].

In 1998, Purdue University reported a SiC accumulation-channel UMOSFET with new structural features that shield the trench oxide from high electric fields in the blocking state [43-44]. The new features consisted of p-type region formed in the trench bottom by self-aligned ion implantation and a thin n-type epilayer incorporated between the n-drift region and the p-type base.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

A way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar implanted DMOSFETs [43-44,27]. Since impurity diffusion is impractical in SiC, the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for the n^+ source. Because p-type implants are conducted at temperatures between1600 and 1700 ^oC, the self-aligned implant process using polysilicon gates is not practical in SiC. Hence, the realignment tolerances must be allowed between two sources and gate. This should also alter the alignment of the underlying base material. Due to these disadvantages, the elimination of the trench corners resulted in a threefold improvement in the device blocking voltage to 760V. This blocking voltage is achieved using 6H-SiC [43-44,27].

In 1998, the 4H-SiC UMOSFET was fabricated with a breakdown voltage of 1.4 kV and a specific on-resistance of 311 $m\Omega cm^2$ by the CREE Research Inc [44]. The fabricated device required the impurity concentration of the drift region of $1x10^{15}/cm^3$ and required n^- thickness of 15μm. For the prototype module, three kinds of 2.0 kV UMOSFETs with different chip areas (0.7x0.7, 1.5x1.5, and 3.0x3.0 mm^2) were designed. All were fabricated in CREE Research Inc by using 4H-SiC wafers. In this report the relationship between the breakdown voltage and the specific on-resistance was presented by various groups which were involved in the fabrication of silicon carbide based power devices.

In 1999, the usefulness of silicon carbide for the device application was explained [45]. In the same year, the theoretical and numerical analysis of SiC JFET and MOSFET at 6.5 kV was presented [46]. According to this report, to improve the on-state/breakdown performance of the JFET, buried layers in conjunction with a highly doped buffer layer have been used. Trench technology has been employed for the MOSFET. The devices are simulated and optimised using MEDICI simulator. In order to obtain a 6.5 kV breakdown voltage, the n-drift region length is 60μm long with a doping concentration of $2x10^{15}$ cm^{-3}. The distance between the gate and the source diffusions is 0.6 μm. For a trench MOSFET, the p-well doping is $5x10^{17}$ cm^{-3} and its length is equal to 3.8 μm. The doping concentration of the n-drift region has to be decreased to $1.7x10^{15}$ cm^{-3}. In order to obtain the proposed breakdown voltage, the n-drift layer length is 60μm long. The gate oxide thickness for the simulated structure is 0.2μm.

In 1999, high-voltage lateral MOSFETs on 6H and 4H SiC wafers were fabricated with 400-475 V breakdown voltage using the RESURF principle [47]. A MOS electron inversion layer mobility of about 50 Ωcm^2/V-sec was obtained on 6H-SiC wafers. This mobility is high enough such that the specific on-resistance of the 6H-SiC MOSFETs is limited by the resistance of the drift layer. The measured FET specific on-resistance $R_{on\text{-}sp}$ ranges from 0.25 to 0.7750 Ωcm^2 depending on the device structure. However, this resistance is much higher than predicted because the sheet resistance of the drift layer is an order of magnitude higher than expected for the implant doses used. This paper also concluded that by redesigning the devices with appropriate drain edge terminations and by reducing gate overlap over the drift region, a substantial increase in breakdown voltage is expected.

In 2000, the characterisation of SiC epitaxial channel MOSFETs was demonstrated. Silicon carbide epitaxial channel MOSFETs were fabricated on 6H SiC substrates with N+ epitaxial source and drain electrodes. The electrical characteristics were modelled in the sub-pinch off depletion and accumulation modes of operation. A buried channel mobility of 230 cm^2/V-sec and an accumulation-

mode surface mobility of 45 cm^2/V-sec were extracted at room temperature under a 50% activation of channel donor impurities [48].

In 2001, high-voltage lateral RESURF metal oxide semiconductor field effect transistors in 4H–SiC were experimentally demonstrated with a breakdown voltage of 900 V and a specific on-resistance of 0.5 Ωcm^2. Lighter RESURF doses and/or thicker gate oxides were required in SiC lateral MOSFETs to achieve highest breakdown voltage capability. In this paper [49], lateral RESURF MOSFETs were fabricated on p/p^+ 4H–SiC substrates with epitaxial thickness and doping of 10µm and $4\text{-}5x10^{15}$ cm^{-3} respectively. The source/drain regions were implanted with phosphorus to create a box profile of junction depth of 0.5µm and total dose of $5x10^{15}$ cm^2. The RESURF region was also realised with a box profile implant of the same junction depth with nitrogen as the dopant. The implants were activated at 1200 ^{0}C in argon ambient.

In 2001, a new 800V lateral MOSFET with dual conduction paths was presented and demonstrated [50]. The feature of this new device was a buried P-type layer that divides the N-type drift region into two parallel conduction paths. The dual conduction paths provide an on-state resistance reduction of 33% as compared to a state-of-the-art double RESURF MOSFET. Charge balance is maintained among the layers to ensure high blocking voltage capability. The manufacturing process was relatively simple and provided excellent control of the charge in each layer by using ion implantation steps rather than epitaxial layers. A new BiCMOS Power IC process featuring this novel device was used to manufacture the cost-effective integrated power supply chips.

In 2001, a 4H-SiC RF power MOSFET was fabricated and characterised for the first time [51]. The improved performance of this device was facilitated by a two-metal-layer process which optimises the conflicting requirements of the acceptable inversion-layer mobility and the low contact resistance. The cut-off frequency of the device with 1µm gate length was in excess of 7 GHz. The breakdown voltage of the newly fabricated MOSFET was found to scale with the drift length. A breakdown voltage of 950 V was achieved in MOSFETs with specific on-resistance of 24 Ωmm^2. The parasitic resistances were reasonably small due to dopant activation and post metallisation anneals. The sheet resistances of the N source/drain and N drift regions were measured to be 300 Ω/sq and 3400 Ω/sq respectively. The resistivity of the ohmic contact was $1.5x10^{-5}$ Ωcm^2.

In 2002, a novel analytical model of a SiC MOSFET was presented [52]. In this paper, by using known experimental results, a semi empirical relation for carrier mobility (µ) dependence on electric field intensity, dopant concentration and temperature was formulated. Based on this relation, appropriate analytical mathematical-physical model for simulation of current-voltage characteristics, transconductance and conductance of MOSFET were developed. All models were formulated taking into account, among other effects, the dependence of threshold voltage on temperature and impurity concentration in the channel, as well as the effect of the channel narrowing. Using the proposed model a simulation algorithm was designed and a simulation of the MOSFET performance was performed.

In 2002, a 10 A, 2.4 kV power DIMOSFET in 4H-SiC was reported and the characteristics of large area (3.3x3.3 mm^2), high-voltage 4H-SiC DiMOSFETs were demonstrated [53]. The MOSFETs showed a peak MOS channel mobility of 22 cm^2/V-sec and a threshold voltage of 8.5 V at room temperature. The DIMOSFETs exhibited an on-resistance of 42 $m\Omega cm^2$ at room temperature and 85 $m\Omega cm^2$ at 200 ºC. Stable avalanche characteristics at approximately 2.4 kV were observed. An on-

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

current of 10 A was measured on a 0.103cm^2 device. High switching speed was also demonstrated. In this paper, the MOS channel length defined by the p-well and n implants was 1.5μm. Electrons flowed laterally from the n source through a MOS channel on the implanted p-well, then flowed vertically through the JFET region formed by two adjacent p-well regions and then through the lightly doped n drift region into the drain. The cell pitch was 16 μm and the packing density of the gate periphery was 1250 cm/cm^2. A 20-μm thick drift layer with a doping concentration of 2.5x10^{15} cm^{-3} was chosen for a 2000 V blocking voltage design. This paper also suggested that the devices are capable of high-voltage, high-frequency and low-loss switching applications.

In 2002, a two-zone, lateral RESURF field 6H-SiC MOSFET with a breakdown voltage as high as 1300 V and a specific on-resistance of 160 m Ωcm^2 was fabricated [54]. These MOSFETs exhibited stable and reversible breakdown indicating an avalanche breakdown in SiC that had not been reported in earlier lateral SiC MOSFETs. In this paper, the device was fabricated on p/p$^+$ 6H-SiC wafers with epitaxial thickness and doping of 10μm and 7x10^{15} cm^{-3} respectively. The specific on-resistance of the MOSFET is lower than any lateral MOSFET reported in silicon or SiC with similar breakdown voltage.

In 2003 and 2004, numerical device simulations on a 4H –SiC vertical MOSFET were presented [55-56]. The simulations mainly focused on reverse blocking voltage, threshold voltage and on-state resistance. The simulated gate MOSFET had a gate oxide thickness of 50nm, a source depth of 0.2 micron and a p-well depth of 1 micron. The channel length was of 1micron.

In 2004, a comparison of modern SiC power devices was demonstrated [57]. In this paper an analysis of the static and dynamic behaviour of a 2 kV SiC MOSFET and IGBT was presented. By comparing the circuit performances it was observed that IGBT is two times faster than MOSFET.

In 2005, a design and fabrication of a 1600V 4H-SiC UMOSFET with a dual buffer layer structure was demonstrated. The fabricated device exhibited 50mΩcm^2 of specific on-resistance with ~1μm of the channel length that could be further reduced to <1μm. In this paper, the n-type drift layer was ~25μm thick with 3-5x10^{15} cm^{-3} of doping concentration. Two n-type buffer layers were grown on top of the drift layer. The first buffer layer was ~3μm thick and 1-2x10^{16} cm^{-3} doped with nitrogen. The second layer was ~0.5μm thick, 0.5-1x10^{17} cm^{-3} doped with nitrogen followed by the final p-type, ~2μm thick base layer with 0.8-1x10^{17} cm^{-3} doped with aluminum. The N$^+$ layer was formed by high energy up to 700 KeV nitrogen implantations to obtain ~1μm channel length [58]. UMOSFET trench gates were perpendicular to the primary flat of the SiC wafers to achieve high inversion channel mobility.

In 2005, an on-state performance of trench oxide-protected SiC UMOSFETs on 115μ m-thick n-type 4H-SiC epilayers designed for blocking voltages up to 14 kV was demonstrated [59]. In this paper, a current density of 137A/cm^2 and a specific on-resistance of 228 mΩcm^2 were achieved at a gate bias of 40 V. The effect of current spreading on the specific on-resistance for finite-dimension devices was investigated. A 115μm-thick, 7.5x10^{14} cm^{-3} n-type epilayer was first grown on n$^+$ 4H-SiC substrate, cut 8^o off axis and followed by a 0.4 μm, 2x10^{17} cm^{-3} n-type current spreading epilayer and a 1.5 μm, 2x10^{17} cm^{-3} p-type epilayer to form the base region of the UMOSFET. Source contacts were formed by implanting 4x10^{15} cm^{-2} nitrogen at 650 ^{o}C using a Ti-Au mask. Gate trenches approximately 2 μm deep were formed by reactive ion etching using a Ni mask. Sacrificial oxidations were performed to smooth the trench sidewalls. The active area of the device was .018cm^2 and required a current 2.5 A. The device required a current density of 137A/cm^2. The blocking layers of doping and the thickness

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

used here were theoretically capable of blocking 14 kV and had actually been demonstrated to block 10 kV. However, problems with the edge terminations in the devices limited the blocking voltage to just over 5 kV [59].

In 2005, a 1330 V, 67mΩcm^2 4H-SiC RESURF lateral MOSFET was investigated [60]. The figure of merit of the presented device was 26 MW/cm^2. This figure of the merit was the best among the reported lateral MOSFETs.

In 2006, 4H-SiC DMOSFETs of breakdown voltages of 1.2 kV and 1.8 kV were fabricated [61]. For 1.2 kV, an epilayer with a doping concentration of 6x10^{15} cm^{-3} and a thickness of 12 μm could be used. For 1.8 kV 4H SiC DMOSFET the device had a gate oxide of 500Å. The gate oxide electric field was limited to approximately 3 MV/cm. The active area of this device was 0.0936 cm^2. An on-resistance of 85 mΩ (R_{on-sp} = 8 mΩcm^2) and a drain current of 50 A (534 A/cm^2) at a forward drop of 5.7 V were measured at room temperature.

In 2006, silicon carbide as energy efficient wide band gap devices was discussed [62]. For RF applications, GaN HEMTs allowed the use of highly efficient Class E circuit topologies demonstrating a high power of 63 W at 2 GHz with 75% power added efficiency. SiC Schottky diodes were allowing up to a 25% reduction in losses in power supplies for computers and servers when used in the power factor correction circuit. Even higher efficiencies could be obtained when the SiC Schottkys were combined with a SiC MOSFET as the switch, resulting in yet another 22% reduction in losses. For motor control, SiC Schottky allowed a >35% reduction in losses as demonstrated for a 3 HP motor drive [62].

In 2007, a compact circuit simulator model was developed and used to describe the performance of a 2kV 4H SiC power DIMOSFET [63]. This model also made a comparison with the widely used 400V, 5A Si power MOSFET. The model's channel current expressions are unique in that they include the channel regions at the corners of square and hexagonal cells that turn on at lower gate voltages and the enhanced linear region transconductance. This model also actively describes the static and dynamic performance of both the Si and SiC devices. In this paper [63] the detailed device comparisons show that both the on-state performance and switching performance at 25 °C are similar between the 400V Si and 2kV SiC MOSFETs with a difference that the SiC device requires twice the gate drive voltage. The main difference between the devices is that the SiC has a five times higher voltage rating without an increase in the specific on-resistance.

Static Induction Transistor

Due to high breakdown field, silicon carbide is an ideal semiconductor for the fabrication of high power microwave devices operating in the 1-10 GHz range. Static induction transistors have power levels of 470 W at 600 MHz and 38 W at 3 GHz. Due to a high thermal conductivity of SiC, it removes the heat from the substrate during microwave operation. Figure 10 shows the cross section of the SiC static induction transistor (SIT). From the cross section it can be observed that the SIT is a majority carrier unipolar device in which the flow of the electrons from source to drain is controlled by a saddle-shaped two-dimensional potential barrier in the semiconductor between the metallic gates. If the doping level and lateral dimensions are chosen correctly, the height of barrier potential will be modulated both by the gate and drain. Since the current increases exponentially as the barrier is lowered, the output characteristics of SIT are like a triode. SIT is important as a microwave device at low frequencies. The

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

maximum drain voltage is 250 V, the on-current at the knee is about 80mA/mm and the blocking gain is approximately 10.

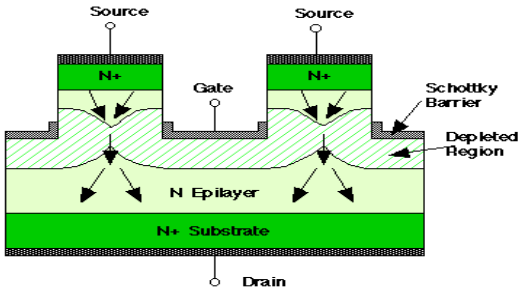

Figure 10. Cross section of static induction transistor (SIT)
(After R. C. Clarke et al., Ref. 64)

Status and issues regarding the analysis and development of SiC based SIT

In 1995, 6H-SiC static induction transistors (SITs) were demonstrated, using SiC-specific semiconductor processing technologies such as VPE, reactive ion etching and self aligned sidewall Schottky gates [64]. Under test conditions, 6H-SiC SITs developed 38 W of output power at 175 MHz, a power added efficiency of 60%, and an associated gain of 10 dB. The maximum channel current was 300 mA, and the maximum blocking voltage was 200 V. SIT requires two extremes of doping, a thick 5µm unintentionally-doped drift layer of $1x10^{16}$ cm^{-3} concentration and a very highly doped ($lx10^{19}$ cm^{-3}), 0.2µm-thick contact layer. The growth chemistry for SiC employs propane as a source of carbon and silane as a source of silicon, transported via hydrogen carrier gas to an inductively heated (1450°C) graphite susceptor [64].

In 1995 also, SITs were demonstrated on 4H SiC [65]. SiC-specific semiconductor processing technologies such as epitaxy, reactive ion etching, and sidewall Schottky gates were employed. Under pulsed power test conditions, 4H-SiC SITs developed a maximum output power of 225 W at 600 MHz, a power added efficiency of 47% and a gain of 8.7 dB. The maximum channel current was 1 A/cm and the maximum blocking voltage was 200 V.

In 1997, solid state DTV transmitters were demonstrated [66]. These transmitters used silicon bipolar, MOS or silicon carbide SIT transistors in the RF power amplifiers. The solid state transmitters achieved the highest power levels by using the latest LDMOS and silicon carbide RF transistors. In 1998, ion implanted SITs in 4H SiC for the microwave power generation in L and S bands were demonstrated. The ion implanted SITs were measured with 35W and 300W output powers at L and S-bands [67]. In 1999, analysis and design of C-band SITs in 4H SiC was demonstrated. Experimental devices were fabricated on n-type epitaxial wafers of 4H-SiC obtained from Cree Research [68].

In 2000, a multiple self-aligned fabrication process was developed for recessed gate microwave SITs in silicon carbide. This process was demonstrated by fabricating 4H-SiC SITs having f_T of 7 GHz [69]. In 2001, a SiC-SIT with SAO structure was fabricated by using aluminum implantation for p gate on 4H n-type SiC [70]. It was found that the SAO structure could be fabricated as expected by observing the cross sectional structure. A very low specific on-resistance of 39 $m\Omega cm^2$ was successfully obtained. By reducing a unit cell, lower on-resistance could be expected.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

In 2002, a vertical channel type static induction transistor with the novel gate structure was introduced [71]. A highest blocking voltage of 2000 V in the case of vertical channel type silicon carbide SITS and a low on-resistance of 70mΩcm^2 were realised. Turn-off characteristics were investigated and a very fast turn-off time of 20 ns at high temperature of 200 ºC under dc voltage of 1000 V was successfully demonstrated. Large current turned-off properties were also demonstrated by a parallel connection of two small SITS. In the same year, a silicon carbide based self-aligned and ion implanted SIT for 150 W having S-band operations got demonstrated [72].

In 2003, the effect of interface charges on the operation of 4H silicon carbide SITs was presented [73].

In 2005, a recessed gate silicon carbide SIT was demonstrated [74]. A developed new approach was used to solve the breakdown voltage and the specific on-resistance and trade-off problem, and consequently an extremely high power capability was achieved. Simulations were fully performed to analyse the influence of critical design parameters on the device power performance. They showed that the basic trade-off was successfully eliminated if the depth of a JFET diffusion layer was greater than 1.35 times the gate trench depth due to the effective suppression of the JFET resistance. Consequently, the proposed device architecture showed much higher power capability than the conventional structure, suggesting that the device power performance be maximised by implementing the JFET diffusion layer in a conventional SiC SIT with a narrow half-width of the source region [74].

In 2006, ultra low on-resistance silicon carbide SITs with buried gate structures (SiC-BGSITs) were successfully developed through an innovative fabrication process [75]. A submicron buried p+ gate structure was fabricated by a combination of submicron trench dry etching and epitaxial growth on a trench structure. The breakdown voltage V_B and specific on-resistance $R_{on\text{-}sp}$ of the fabricated SiC-BGSIT were 700V at a gate voltage $V_G = -12$ V, and 1.0 mΩcm^2 at a current density of $J_D = 200$ A/cm^2 and $V_G = 2.5$ V respectively. This $R_{on\text{-}sp}$ was the lowest on-resistance for 600V-class power switching devices, including other SiC devices and GaN HEMTs. The fabricated BGSIT with N_{ch} was $1.3\text{x}10^{16}$ /cm^3. The device active area and W_{ch} were 200x200 μm^2 and 0.9 μm respectively. The drain current I_D reached 0.08 A, corresponding to a current density J_D of 200 A/cm^2 at a drain voltage $V_D = 0.2$ V and $V_G = 2.5$ V. From these parameters, the calculated $R_{on\text{-}sp}$ was as low as 1.0 mΩ cm^2. The $R_{on\text{-}sp}$ calculated by the device simulator of the same dimension as the fabricated device was 1.1 mΩcm^2, which was almost the same as the measured $R_{on\text{-}sp}$. From the characteristics, we can observe the decrease of the drain-current I_D at $V_D > 6$ V. This phenomenon probably comes from the decrease of the carrier mobility by the self-heating effect and implies the thermal and electrical hardness of such a device at high current density.

In 2007, a buried gate SIT in 4H-SiC with ultra low on-resistance was presented [76]. A result of device simulation showed the appropriate parameters for the device design. For BGSIT with wide W_{ch}, an ultra-low $R_{on\text{-}sp}$ of 1.1 mΩcm^2 was obtained with normally-on characteristic, while a clear saturation I_{DS}-V_{DS} characteristic and a slightly high $R_{on\text{-}sp}$ of 1.4 mΩcm^2 were obtained with quasi normally-off characteristic for BGSIT with narrow W_{ch}. In order to realise normally-off characteristic, W_{ch} must be reduced more. However, it must be realised without increase of on-resistance.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Nonvolatile Memory

The wide bandgap of SiC results in an extremely low value of the intrinsic carrier concentration at room temperature, which is lower than that due to silicon. The leakage current of SiC is negligible. Hence the dynamic memory cells in SiC have storage times of many years at room temperature. Figure 11 shows the cross section of SiC vertically integrated bipolar NVRAM cell at left along with N-channel MOSFET control logic at right. The NVRAM cell consists of an NPN bipolar access transistor connected to a pn junction storage capacitor. Storage times are plotted as a function of temperature. If these data are extrapolated to lower temperatures, they predict a room temperature storage time of over one million years and give the concept of a truly nonvolatile memory [77].

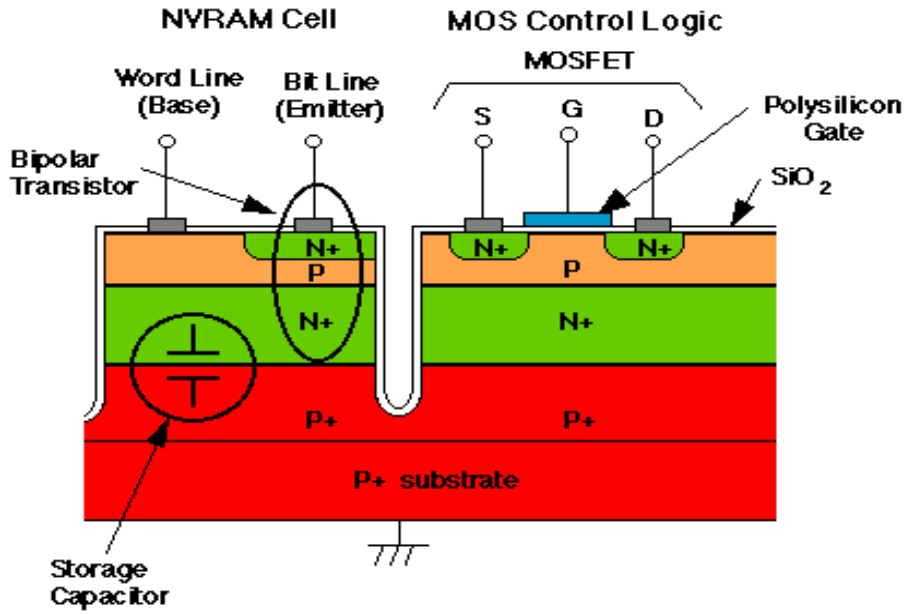

Figure 11. Cross section of nonvolatile memory
(After J. A. Copper, Jr. et al., Ref. 77)

Status and issues regarding the analysis and development of SiC based nonvolatile memory

In a paper on dynamic charge storage in 6H silicon carbide presented in 1992 [78], pn-junction storage capacitors were fabricated in 6H silicon carbide. The charge decay was dominated by surface generation at the mesa edges and the storage time strongly depended on the method of surface passivation. Charge recovery was thermally activated. Devices passivated by dry oxidation and by wet oxidation exhibited activation energies of 0.66 and 1.48 eV respectively. As a figure of merit, extrapolation of the dry-oxide data gave a room-temperature storage time of 10^6 s, while the same operation on the wet-oxide data gave a value of 10^{14} s.

In 1994, a vertically integrated bipolar storage cell in 6H silicon carbide for nonvolatile memory applications was reported [79]. The vertically integrated 6H-SiC bipolar memory cell had an extrapolated room-temperature storage time of 10^6 s. Electrical writing of the cell was demonstrated.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

Since no applied bias was needed during the storage state, the bipolar cell had a potential for use as a nonvolatile memory.

In the same year, the first monolithic NMOS digital integrated circuits in 6H-SiC were presented [80]. The logic gates were implemented in enhancement-mode NMOS using ion implanted MOSFETs with non-self-aligned metal gates. Inverters, NAND and NOR gates, XNOR gates, D-latches, RS flip-flops, binary counters, and half adders were fabricated and characterised. All circuits operated properly from room temperature to over 300°C.

In 2001, N_2O and NO nitridation by either annealing or direct growth of gate oxides on 4H SiC were analysed [81]. The analysis was based on binding energies from x-ray photoelectron spectroscopy and depth profiles of nitrogen at the SiO_2-SiC interface from secondary ion mass spectrometry. A clean SiO_2-SiC interface was found in both NO and N_2O annealed/grown samples as opposed to the interface annealed in Ar which exhibited complex sub-oxides and oxide-carbon compounds.

In 2002, nonvolatile memory characteristics of MOS capacitors were presented [82]. The MOS capacitors were fabricated on N-type 4H SiC substrate with nitrided oxide-semiconductor interface. The charge-retention time was in the order of 4.6×10^9 years as determined by thermally activated (275-355ºC) capacitance transient measurements and extrapolation to room temperature. The estimated activation energy of the charge generation processes was 1.6 eV. The results and the analysis demonstrate that 4H SiC MOS capacitors can be used as a memory element in nonvolatile RAMs.

Conclusions

At present SiC devices appear to compete in the semiconductor market as high voltage, high power switching devices. In this paper we estimate that SiC can be used as a power device and in the development of the nonvolatile memory. It has also been examined that SiC devices can also be operated at microwave frequencies. However, in order to become economically feasible, several critical materials and processing issues still need to be solved.

References

1. J. A. Lely, "Darstellung von einkristallen von siliziumcarbid und beherrschung von art and menge der eingebauten verunreinigungen," *Ber. Dt. Kerm. Ges.*, **1955**, *32*, 229-231.
2. Y. M. Tairov and V. F. Tsvetkov, "Investigations of growth processes of ingots of silicon carbide single crystals," *J. Cryst. Growth,* **1978**, *43*, 209-212.
3. G. Ziegler, P. Lanig, D. Theis, and C. Weyrich, "Single crystal growth of SiC substrate material for blue light emitting diodes," *IEEE Trans. Electron Devices*, **1983**, *30*, 277-281.
4. C. H. Carter, Jr., L. Tang and R. F. Davis, "Growth and characterization of silicon carbide crystal", 4th National Review Meeting on the Growth and Characterization of Silicon Carbide, Raleigh, NC, USA, **1987**, pp.15-28.
5. M. Ostling and N. Lundberg, **"**Low ohmic cobalt silicide contacts to p-type 6H-SiC", IEEE Device Research Conf., Santa Barbara, CA, USA, June **1996**, pp.157-157.
6. S. Sridevan, P. K. Mclarty, and B. J. Baliga, "On the presence of aluminum in thermally grown oxides on 6H-silicon carbide [power MOSFETs]", *IEEE Electron Device Lett.*, **1996**, *17*, 136-138.

7. J. W. Palmour, Cree Research, private communication, **1996.**
8. R. Y. Lakshman, "A Process for hydrogenation of silicon carbide crystals", *MS. Thesis*, **2001**, Mississipi State University, USA.
9. A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blocking characteristics of high-voltage 4H-SiC Schottky rectifiers with boron-implanted edge termination", *IEEE Electron Device Lett.*, **1996**, *17*, 139-141.
10. C. Weitzel, J. Palmour, C. Carter, K. Moore, K. Nordquist, S. Allen, C. Thero, and M. Bhatnagar, "Silicon carbide high-power devices", *IEEE Trans. Electron Devices*, **1996**, *43*, 1732-1741.
11. D. Alok and B. J. Baliga, "SiC device edge termination using finite area argon implantation", *IEEE Trans. Electron Devices*, **1997**, *44*, 1013-1017.
12. G. Brezeanu, M. Badila, B. Tudor, and B. Millan, "Accurate modeling of Ni/6H SiC Schottky barrier diode (SBD) forward characteristics at high current densities", Int. Conference on Semiconductor, Sinaia, Romania, October **2000,** Vol.1, pp. 193-196.
13. D. T. Morisette, J. A. Cooper, Jr., M. R. Melloch, G. M. Dolny, P. M. Shenoy, M. Zafrani, and J. Gladish, "Static and dynamic characterization of large area high-current-density SiC Schottky diodes", *IEEE Trans. Electron Devices*, **2001**, *48*, 349-352.
14. B. Gheorghe, M. Badila, B. Tudor, J. Millan, P. Godignon, F. Udrea, G. A. J. Amaratunga, and A. Mihaila, "Accurate modeling and parameter extraction for 6H-SiC Schottky barrier diodes (SBDs) with nearly ideal breakdown voltage", *IEEE Trans. Electron Devices*, **2001**, *48*, 2148-2153.
15. Z. Liu, S. Wang, F. Yu, Y. Zhang, and H. Zhao, "Ti Schottky barrier diodes on n-type 6H-SiC", 6th Int. Conference on Solid State and Integrated Circuit Technology, Beijing, China, October **2001**, Vol. 2, pp. 1183-1186**.**
16. K. Kinoshita, T. Hatakeyama, O. Takikawa, A. Yahata, and T. Shinohe, "Guard ring assisted RESURF: A new termination structure providing stable and high breakdown voltage for SiC power devices", 14th Int. Symposium on Power Semiconductor Devices and ICs, Santa Fe, NM, USA, June **2002**, pp. 253-256.
17. J. H. Zhao, P. Alexandrov, and X. Li, "Demonstration of the first 10-kV 4H-SiC Schottky barrier diodes", *IEEE Trans. Electron Device Lett.,* **2003**, *24*, 402-404.
18. Y. Zhang, Y. Zhang, Y. Wang, and R. Liang, "The effect of different mechanism on the characteristics of SiC Schottky barrier diode", 4th Int. Workshop on Junction Technology, Beijing, China, March **2004**, pp. 171-174.
19. T. Nakamura, T. Miyanagi, I. Kamata, T. Jikimoto, and H. Tsuchida, "A 4.15 kV, 9.07mΩcm^2 4H–SiC Schottky barrier diode using Mo contact annealed at high temperature", *IEEE Trans. Electron Device Lett.*, **2005**, *26*, 99-101.
20. X. Jordan, D. Fournier, M. Vellvehi, A. P Crez, R. Perez, P. Godignon, and J. Millin, "Comparative evaluation of high current SiC Schottky diodes and Si PN junction diodes", Spanish Conference on Electron Devices, Tarragona, Barcelona, Spain, February **2005,** pp.87-90.
21. C. H. Zhou, X. R. Luo, X. C. Deng, J. P. Zhang, Z. J. Li, and B. Zhang,"High breakdown voltage 4H-SiC Schottky barrier diodes with floating metal rings for MMIC applications", 8th Int. Conference on Solid-State Integrated Circuit Technology, Shanghai, China, October **2006**, pp. 944-946.
22. S. Hu and K. Shan, "A new edge termination technique for SiC power devices", *Solid State Electronics*, **2004**, *48*, 122-123.
23. J. A. Cooper, M. R. Melloch, R. Singh, A. Aggarwal, and J. W. Palmour, "Status and prospect for SiC MOSFET", *IEEE Trans. Electron Devices*, **2002**, *49*, 658-664.
24. R. Kosugi, S. Suzuki, M. Okamoto, S. Harada, J. Senzaki, and K. Fukuda, "Strong dependence of the inversion channel mobility of 4H and 6H SiC (0001) MOSFETs on the water content in pyrogenic re-oxidation annealing", *IEEE Electron Device Lett.*, **2002**, *23*, 136-138.
25. S. M. Sze, "Physics of Semiconductor Devices," 2nd Edn., John Wily & Sons, New York, **1985**.

26. J. N. Shenoy, J. A. Cooper, and M. R. Melloch, "High-voltage double-implanted MOS power transistors in 6H-SiC", IEEE Device Research Conference, Santa Barbara, CA, USA, June **1996**, pp. 202-204.
27. J. N. Shenoy, J. A. Cooper, and M. R. Melloch, "High-voltage double-implanted power MOSFET's in 6H-SiC," *IEEE Trans. Electron Device Lett.*, **1997**, *18*, 93-95.
28. P. M. Shenoy and B. J. Baliga, "The planar 6H-SiC ACCFET: A new high-voltage power MOSFET structure," *IEEE Trans. Electron Device Lett.*, **1997**, *18*, 589-591.
29. M. Ruff, H. Mitlehner, and R. Helbig, "SiC devices: Physics and numerical simulation", *IEEE Trans . Electron Device*, **1994**, *41*, 1040-1054.
30. M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC and Si for power devices", *IEEE Trans. Electron Devices*, **1993,** *40*, 645-655.
31. K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high power electronics," *IEEE Trans. Electron Devices*, **1989**, *36*, 1811-1823.
32. B. J. Baliga, "Trends in power semiconductor devices," *IEEE Trans. Electron Devices*, **1996**, *43*, 1717-1731.
33. R. B. Hillborn and H. Kang, "Charge Carrier Concentration and Mobility in n-Type 6H Polytypes of SiC", University of South Carolina Press, **1973**, pp. 337-339.
34. J. Tan, J. A. Cooper, Jr., and M. R. Melloch, "High-voltage accumulation-layer UMOSFETs in 4H SiC", *IEEE Electron Device Lett.*, **1998**, *19*, 487-489.
35. J. Spitz, J. A. Cooper, and M. R. Melloch, "High-voltage lateral DMOSFETs in 4H-SiC", *IEEE Electron Device Lett.*, **1998**, *19*, 100-102.
36. B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications", *IEEE Electron Device Lett.*, **1989**, *10*, 455-457.
37. D. M. Brown, M. Ghezzo, J. Kretchmer, E. Downey, J. Pimbley, and J. Palmour, "SiC MOS interface characteristics", *IEEE Trans. Electron Devices*, **1994**, *41*, 618-620.
38. J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., "Vertical power devices in silicon carbide," Int. Conference on Silicon Carbide and Related Materials, Santa Barbara, USA, **1994**, p. 499.
39. A. K. Agarwal, R. R. Siergiej, S. Seshadri, M. H. White, P. G. McMullin, A. A. Burk, L. B. Rowland, C. D. Brandt, and R. H. Hopkins, "A critical look at the performance advantages and limitations of 4H-SiC power UMOSFET structures", 8th Int. Symposium on Power Semiconductor Devices and ICs, Maui, HI, USA, May **1996**, pp. 119-122.
40. A. K. Agarwal, J. B. Cascady, L. B. Rowland, W. F. Valek, M. H. White, and C. D. Brandt, "1.1KV 4H-SiC Power UMOSFET's," *IEEE Trans. Electron Device Lett.*, **1997**, *18*, 586-588.
41. Y. Sugawara and K. Asano, "1.4 kV 4H-SiC UMOSFET with low specific on resistance," Int. Symposium on Power Semiconductor Devices and ICs, Kyoto, Japan, **1998**, pp.119-122.
42. J. B. Casdy, A. K. Agarwal, L. B. Rowland, W. F. Valek, and C. D. Brandt, "900V DMOS and 1100 V UMOS 4H-SiC power FET's," IEEE Devices Research Conference, Fort Collins, USA, June **1997**, pp. 32-33.
43. J. B. Casady, A. K. Agarwal, L. B. Rowland, S. Seshadri, P. A. Sanger, and C. D. Brandt, "Silicon carbide MOSFET technology", IEEE Int. Symposium on Compound Semiconductor, San Diego, USA, **1997**, pp. 359-362 .
44. Y. Sugawara and K. Asan, "1.4kV 4H-SiC UMOSFET with low specific on- resistance", 10th Int. Symposium on Power Semiconductor Devices and ICs, Kyoto, Japan, June **1998**, pp.119-122.
45. C. M. Johnson, N. G. Wright, S. Ortolland, D. Morrison, K. Adachi, and A. O'Neill, "Silicon carbide power devices: hopeful or hopeless?", IEE Colloquium on Recent Advances in Power Devices, London, UK, **1999**, pp. 10/1-10/5.

46. A. Mihaila, F. Udrea, R. Azar, J. Liang, G. Amaratungal, A. Rusu, and G. Brezeanu, "Theoretical and numerical investigation of SiC JFET and MOSFET at 6.5kV", Semiconductor Conference, Sinaia, Romania, October **1999**, pp.191-194**.**
47. N. S. Saks, S. S. Mani, A. K. Agarwal, and M. G. Ancona, "A 475-V high-voltage 6H-SiC lateral MOSFET", *IEEE Electron Device Lett.*, **1999**, *20*, 431-433.
48. W. E. Wagner, III and M. H. White, "Characterization of silicon carbide epitaxial channel MOSFETs", *IEEE Trans. Electron Devices*, **2000**, *47*, 2214-2220.
49. S. Banerjee, K. Chatty, T. P. Chow, and R. J. Gutmann, "Improved high-voltage lateral RESURF MOSFETs in 4H–SiC", *IEEE Electron Device Lett.*, **2001**, *22*, 209-211.
50. D. R. Disney, A. K. Paul, M. Darwish, R. Basecki, and V. Rumennik, "A new 800V lateral MOSFET with dual conduction paths", Int. Symposium on Power Semiconductor Devices and ICs, Osaka, Japan, **2001**, pp. 399-402.
51. D. Alok, E. Arnold, R. Egloff, J. Barone, J. Murphy, R. Conrad, and J. Burke, "4H-SiC RF power MOSFETs", *IEEE Electron Device Lett.*, **2001**, *22*, 577-578.
52. R. Ramovi, M. Jevti, J. Hadzi-Vukovi, and D. Randjelov, "A novel analytical model of a SiC MOSFET", 23rd Int. Conference on Microelectronics (MIEL 2002), Nis, Yugoslavia, May **2002**, Vol. 2, pp. 447-450.
53. S. H. Ryu , A. Agarwal, J. Richmond, J. Palmour, N. Saks, and J. Williams, "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC", *IEEE Electron Device Lett.*, **2002**, *23*, 321-323.
54. S. Banerjee, T. P. Chow, and R. J. Gutmann, "1300-V 6H-SiC Lateral MOSFETs with two RESURF zones", *IEEE Electron Device Lett.*, **2002**, *23*, 624-626.
55. M. Hasanuzzaman, S. K. Islam, and L. M. Tolbert, "Model simulation and verification of vertical double implanted (DIMOSFET) transistor in 6H-SIC", *Int. J. Modeling and Simulation*, **2003**, *4*, 1-4.
56. M. Avram, G. Brezeanu, and D. P. Poenar, "The comparison of modern SiC power devices", IEEE Int. Conference on Industrial Technology, Hammamet, Tunisia, December **2004**, Vol.1, pp.504-509.
57. L. Chen, O. J. Guy, M. R.Jennings, S. P. Wilks, and P. A. Mawby, "Simulation study of 1.2kV 4H-SiC DIMOSFET structures", 7th Int. Conference on Solid-State and Integrated Circuits Technology, Beijing, China, October **2004**, Vol.3, pp. 2341-2344.
58. Q. Zhang, M. Gomez, C. Bui, and E. Hanna, "1600V 4H-SiC UMOSFETs with dual buffer layers", 17th Int. Symposium on Power Semiconductor Devices and IC's", Santa Barbara, CA, USA, May **2005**, pp. 211-214.
59. Y. Sui, T. Tsuji, and J. A. Cooper, Jr., "On-state characteristics of SiC power UMOSFETs on 115 μm drift layers", *IEEE Electron Device Lett.*, **2005**, *26*, 255-257.
60. T. Kimoto, H. Kawano, and J. Suda, "1330 V, 67 mΩ cm^2 4H-SiC (0001) RESURF MOSFET", *IEEE Electron Device Lett.*, **2005**, *26*, 649-651.
61. A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S. H. Ryu, and J. Zhang, "Progress in silicon carbide power devices", 64th Device Research Conference, Pennsylvania, USA, June **2006**, pp. 155-158.
62. J. W. Palmour, "Energy efficient wide bandgap devices", Compound Semiconductor Integrated Circuit Symposium 2006, San Antonio, TX, USA, November **2006**, pp. 4-7.
63. T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, "Silicon carbide power MOSFET model and parameter extraction sequence", *IEEE Trans. Power Electronics*, **2007**, *22*, 353-362.
64. R. C. Clarke, R. R. Siergiej, A. K. Agarwal, C. D. Brandt, A. A. Burk, Jr., A. Morse, and P. A. Orphanos, "30W VHF 6H-SiC Power static induction transistor", IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, USA, August **1995**, pp. 47-55.

65. R. C. Clarke, R. R. Siergiej, A. K. Agarwal, C. D. Brandt, A. A. Burk, Jr., A. Morse, and P. A. Orphanos, "High power 4H SiC static induction transistors", Int. Electron Devices Meeting, Washington, DC, USA, December **2005**, pp. 353-356.
66. C. Davis, J. Hawkins, and C. Einolf, Jr.,"Solid state DTV transmitters", *IEEE Trans. Broadcasting*, **1997**, *43*, 252-260.
67. A. K. Agarwal, L. S. Chen, G. W. Eldridge, R. R. Siergiej, and R. C. Clarke, "Ion-implanted static induction transistors in 4H-SiC", 56th Device Research Conference, Charlottesville, VA, USA, June **1998**, pp. 94-95.
68. J. P. Henning, A. Przadka, M. R. Melloch, and J. A. Cooper, Jr., "Design and demonstration of C-band static induction transistors in 4H silicon carbide", 57th Device Research Conference, Santa Barbara, CA, USA, June **1999**, pp. 26-28.
69. J. P. Henning, A. Przadka, M. R. Melloch, and J. A. Cooper, Jr., "A novel self-aligned fabrication process for microwave static induction transistors in silicon carbide", *IEEE Electron Device Lett*., **2000**, *21*, 578-580.
70. H. Onose, T. Yatsuo, A. Watanabe, T. Yokota, T. Ishikawa, I. Sanpei, T. Someya, and Y. Kobayashi, "Design consideration for 2 kV SiC-SIT", 13th Int. Symposium on Power Semiconductor Devices and IC's", Osaka, Japan, June **2001**, pp. 179-182.
71. H. Onose, A. Watanabe, T. Someya, and Y. Kobayashil, "Switching properties of 2 kV SiC- SIT", 14th Int. Symposium on Power Semiconductor Devices and IC's, Santa Fe, NM, USA, June **2002**, pp. 134-135.
72. T. J. Knight, R. C. Clarke, R. R. Barron, J. A. Ostop, B. A. Morick, J. R. Gigante, W. J. Malkowski, A. W. Morse, G. DeSalvo, and K. J. Petrosky, "A silicon carbide self-aligned and ion implanted static induction transistor (SAI-SIT) for 150 watt S-band operation", 60th Device Research Conference, Santa Barbara, California, USA, June **2002**, pp.179-180.
73. J. Fuerherm, Y. A. Zeng, and M. H. White, "A study of interface charges on the operation of 4H silicon carbide (SiC) static induction transistors", Int. Symposium on Semiconductor Device Research, Washington, DC, USA, December **2003**, pp. 134-135.
74. Y. C. Choi, H. Y. Cha, M. Chandrasekhar, L. F. Eastman, and M. G. Spencer, "A new approach to maximizing the power handling capability in recessed-gate silicon carbide static induction transistors", IEEE 36th Power Electronics Specialist Conference, Orlando, FL, USA, **2005**, pp. 2171-2174.
75. Y. Tanaka, M. Okamoto, A. Takatsuka, K. Arai, T. Yatsuo, K. Yano, and M. Kasuga, "700-V, 1.0-mΩcm^2 Buried gate SiC-SIT", *IEEE Electron Device Lett.*, **2006**, *27*, 908-910.
76. Y. Tanaka, M. Okamoto, A. Takatsuka, K. Arai, T. Yatsuo, K. Yano, and M. Kasuga, "Buried gate static induction transistors in 4H-SiC (SiC-BGSITs) with ultra low on-resistance, 19th Int. Symposium on Power Semiconductor Devices and ICs, Jeju, Korea, May **2007**, pp. 93-96.
77. J. A. Cooper, Jr., J. W. Palmour, C. T. Gardner, M. R. Melloch, and C. H. Carter, Jr., "Bulk and perimeter generation in 6H-SiC diodes," Int. Semiconductor Device Research Symposium, Charlottesville, VA, USA, December **1991**, pp. 110-112.
78. J. A. Cooper, Jr., M. R. Melloch, W. Xie, J. A. Palmour, and C. H. Carter, Jr., "Dynamic charge storage in 6H-silicon carbide: prospects for high-speed nonvolatile RAM's," *IEEE Trans. Electron Devices*, **1992**, *39*, 2646-2647.
79. W. Xie, J. A. Cooper, Jr., M. R. Melloch, J. W. Palmour, and C. H. Carter, Jr, "A vertically integrated bipolar storage cell in 6H silicon carbide for nonvolatile memory applications", *IEEE Electron Device Lett.*, **1994**, *15*, 212-214.
80. W. Xie, J. A. Cooper, Jr., and M. R. Melloch, "Monolithic NMOS digital integrated circuits in 6H-SiC", *IEEE Electron Device Lett.*, **1994**, *15*, 455-457.
81. P. Jamet and S. Dimitrijev, "Physical properties of N_2O and NO-nitrided gate oxides grown on 4H SiC," *Appl. Physics Lett.*, **2001**, *79*, 323–325.

Mj. Int. J. Sci. Tech. **2008**, *2*(03), 444-470

82. K. Y. Cheong and S. Dimitrijev, "MOS capacitor on 4H–SiC as a nonvolatile memory element", *IEEE Electron Device Lett.*, **2002**, *23*, 404-406.
83. J. Spitz, J. A. Cooper, and M. R. Melloch, "Lateral power MOSFETs", http://www.ecn.purdue.edu/wbg/DeviceResearch/LDMOSFETs/Index.html, Purdue WBC, Purdue University, West Lafayette, IN, USA, July **1997**.
84. www.ece.rutgers.edu/~jzhao, **1992**.